

MEMORY

CMOS 2M × 64**FAST PAGE MODE DRAM MODULE****MB8502D064AA-60/-70****CMOS 2M × 64 Bit Fast Page Mode DRAM Module****DESCRIPTION**

The Fujitsu MB8502D064AA is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117800A devices. The MB8502D064AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8502D064AA are the same as the MB8117800A which features fast page mode operation. For ease of memory expansion, the MB8502D064AA is offered in an 168-pad Dual In-line Memory Module package (DIMM).

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	V
Input Voltage	V _{IN}	-0.5 to +7.0	V
Output Voltage	V _{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I _{OUT}	50	mA
Power Dissipation	P _D	10	W
Storage Temperature	T _{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

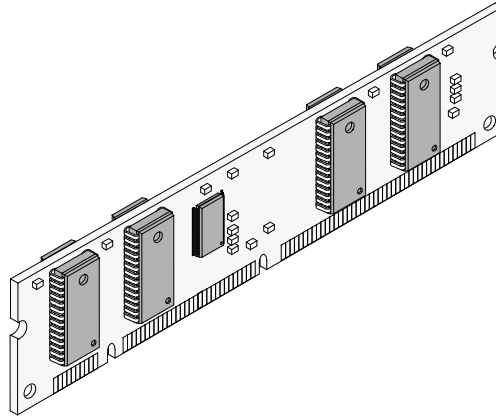
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Parameter		MB8502D064AA-60	MB8502D064AA-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		110 ns max.	130 ns max.
Address Access Time		35 ns max.	40 ns max.
CAS Access Time		20 ns min.	22 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Power Dissipation	Operating Mode	6600 mW max.	6105 mW max.
	Standby Mode	440 mW max.	440 mW max.

- Conformed to 8-Byte DIMM JEDEC standard
- Organization : 2,097,152 words × 64 bits
- Module Size : 1.00" (height) × 5.25" (length) × 0.350" (thick)
- Memory : MB8117800A (2M × 8, 2K ref.), 8 pcs
- TI's Input Buffers, 2 pcs
- TI's Input Driver for Buffered PD, 1pc
- Decoupling Capacitors, 10 pcs
- 5.0 V ± 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Fast Page operation
- RAS Only Refresh / CAS-before-RAS Refresh
- Package and Ordering Information:
168-pad DIMM, order as
MB8502D064AA-xxDG (DG = Gold Pad)

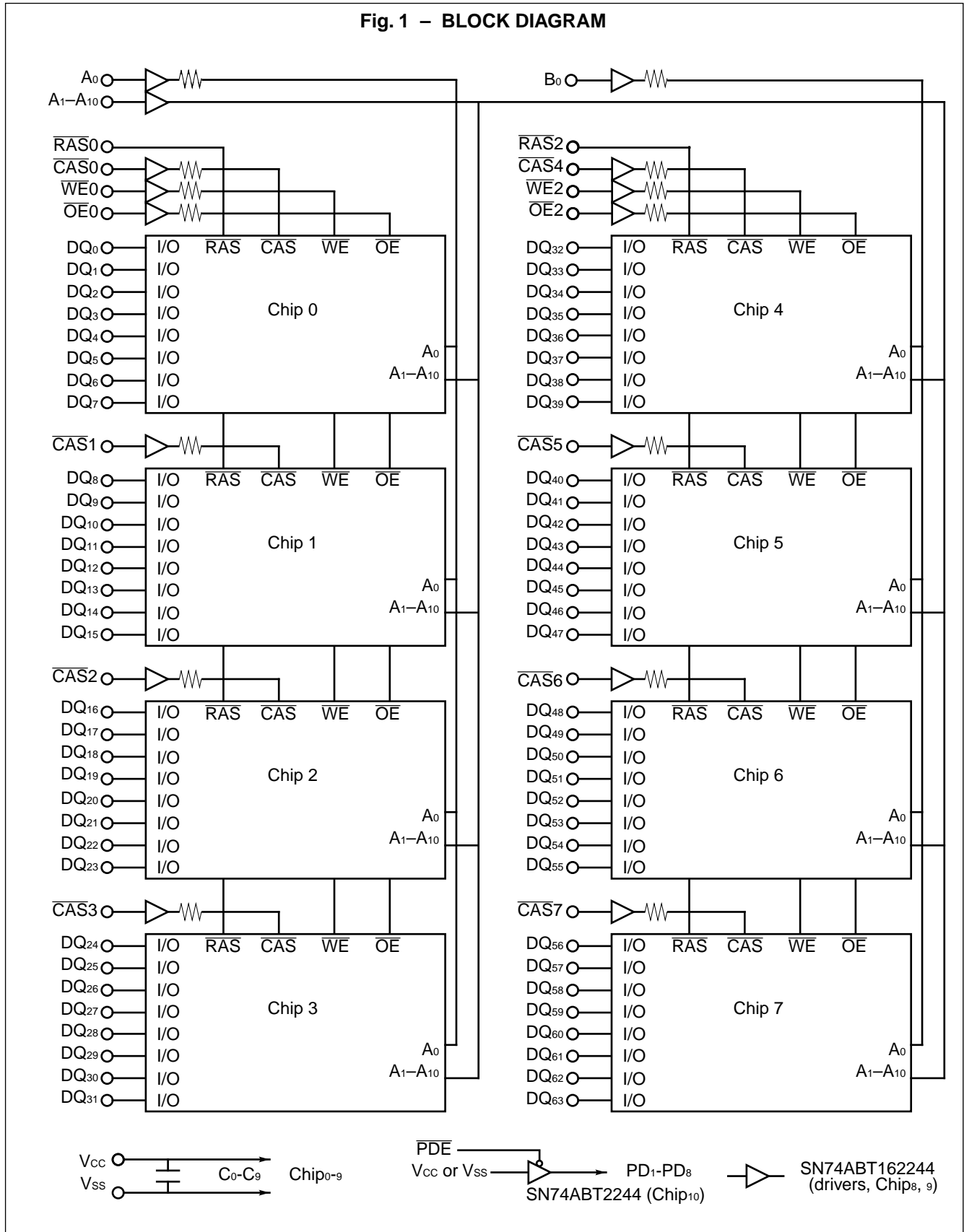
■ PACKAGE



MDS-168P-P06

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Fig. 1 - BLOCK DIAGRAM



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■ PIN ASSIGNMENTS

Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA
1	V _{SS}	36	A ₆	71	DQ ₂₇	106	NC
2	DQ ₀	37	A ₈	72	DQ ₂₈	107	V _{SS}
3	DQ ₁	38	A ₁₀	73	V _{CC}	108	NC
4	DQ ₂	39	NC	74	DQ ₂₉	109	NC
5	DQ ₃	40	V _{CC}	75	DQ ₃₀	110	V _{CC}
6	V _{CC}	41	NC	76	DQ ₃₁	111	NC
7	DQ ₄	42	NC	77	NC	112	$\overline{\text{CAS}}1$
8	DQ ₅	43	V _{SS}	78	V _{SS}	113	$\overline{\text{CAS}}3$
9	DQ ₆	44	$\overline{\text{OE}}2$	79	PD ₁	114	NC
10	DQ ₇	45	$\overline{\text{RAS}}2$	80	PD ₃	115	NC
11	NC	46	$\overline{\text{CAS}}4$	81	PD ₅	116	V _{SS}
12	V _{SS}	47	$\overline{\text{CAS}}6$	82	PD ₇	117	A ₁
13	DQ ₈	48	$\overline{\text{WE}}2$	83	ID ₀	118	A ₃
14	DQ ₉	49	V _{CC}	84	V _{CC}	119	A ₅
15	DQ ₁₀	50	NC	85	V _{SS}	120	A ₇
16	DQ ₁₁	51	NC	86	DQ ₃₂	121	A ₉
17	DQ ₁₂	52	DQ ₁₆	87	DQ ₃₃	122	NC
18	V _{CC}	53	DQ ₁₇	88	DQ ₃₄	123	NC
19	DQ ₁₃	54	V _{SS}	89	DQ ₃₅	124	V _{CC}
20	DQ ₁₄	55	DQ ₁₈	90	V _{CC}	125	NC
21	DQ ₁₅	56	DQ ₁₉	91	DQ ₃₆	126	B ₀
22	NC	57	DQ ₂₀	92	DQ ₃₇	127	V _{SS}
23	V _{SS}	58	DQ ₂₁	93	DQ ₃₈	128	NC
24	NC	59	V _{CC}	94	DQ ₃₉	129	NC
25	NC	60	DQ ₂₂	95	NC	130	$\overline{\text{CAS}}5$
26	V _{CC}	61	NC	96	V _{SS}	131	$\overline{\text{CAS}}7$
27	$\overline{\text{WE}}0$	62	NC	97	DQ ₄₀	132	$\overline{\text{PDE}}$
28	$\overline{\text{CAS}}0$	63	NC	98	DQ ₄₁	133	V _{CC}
29	$\overline{\text{CAS}}2$	64	NC	99	DQ ₄₂	134	NC
30	$\overline{\text{RAS}}0$	65	DQ ₂₃	100	DQ ₄₃	135	NC
31	$\overline{\text{OE}}0$	66	NC	101	DQ ₄₄	136	DQ ₄₈
32	V _{SS}	67	DQ ₂₄	102	V _{CC}	137	DQ ₄₉
33	A ₀	68	V _{SS}	103	DQ ₄₅	138	V _{SS}
34	A ₂	69	DQ ₂₅	104	DQ ₄₆	139	DQ ₅₀
35	A ₄	70	DQ ₂₆	105	DQ ₄₇	140	DQ ₅₁

(Continued)

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(Continued)

Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA
141	DQ ₅₂	148	NC	155	DQ ₅₉	162	V _{SS}
142	DQ ₅₃	149	DQ ₅₅	156	DQ ₆₀	163	PD ₂
143	V _{CC}	150	NC	157	V _{CC}	164	PD ₄
144	DQ ₅₄	151	DQ ₅₆	158	DQ ₆₁	165	PD ₆
145	NC	152	V _{SS}	159	DQ ₆₂	166	PD ₈
146	NC	153	DQ ₅₇	160	DQ ₆₃	167	ID ₁
147	NC	154	DQ ₅₈	161	NC	168	V _{CC}

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■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A ₀ to A ₁₀ , B ₀	Address Input	Input	12
$\overline{\text{RAS}}_0$ and $\overline{\text{RAS}}_2$	Row Address Strobe	Input	2
$\overline{\text{CAS}}_0$ to $\overline{\text{CAS}}_7$	Column Address Strobe	Input	8
$\overline{\text{WE}}_0$ and $\overline{\text{WE}}_2$	Write Enable	Input	2
$\overline{\text{OE}}_0$ and $\overline{\text{OE}}_2$	Output Enable	Input	2
DQ ₀ to DQ ₆₃	Data-input/Data-output	Input/Output	64
PD ₁ to PD ₈	Presence Detect	Output	8
ID ₀ and ID ₁	ID bit	Output	2
$\overline{\text{PDE}}$	Presence Detect Enable	Input	1
V _{CC}	Power Supply	—	16
V _{SS}	Ground	—	16
NC	No Connection	—	35

■ PRESENCE DETECT (PD)/ID DEFINITION

Symbol	MB8502D064AA-60	MB8502D064AA-70	Description of PD/ID
PD ₁	H	H	MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING; Module Density: 16MB, Number of Bank: 1 Bank Module Configuration: 2M × 64 Mounted DRAM Configuration: 2M × 8 DRAM Address (Row/Column): 11/10
PD ₂	L	L	
PD ₃	L	L	
PD ₄	H	H	
PD ₅	L	L	EDO DETECTION; Fast Page Mode : PD ₅ = L
PD ₆	H	L	MODULE SPEED; 60 ns : PD ₆ = H, PD ₇ = H 70 ns : PD ₆ = L, PD ₇ = H
PD ₇	H	H	
PD ₈	H	H	ECC / PARITY DETECTION; (parity) : PD ₈ = H
ID ₀	L	L	MODULE TYPE; ×64 (parity) : ID ₀ = L
ID ₁	H	H	REFRESH MODE; Self Refresh : ID ₁ = L

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = +5.0 V)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance, (Address)	C _{IN1}	—	20	pF
Input Capacitance ($\overline{\text{RAS}}$)	C _{IN2}	—	50	pF
Input Capacitance, ($\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{IN3}	—	20	pF
I/O Capacitance, (DQ)	C _{DQ}	—	20	pF

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■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.0	V
Input Low Voltage, all inputs*	V_{IL}	-0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

Note: *Undershoots of up to -1.5 volts with a pulse width not exceeding 10 ns are acceptable.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min.	Max.	Unit
Output High Voltage* ¹	$I_{OH} = -5 \text{ mA}$	V_{OH}	2.4	—	V
Output Low Voltage* ¹	$I_{OL} = 4.2 \text{ mA}$	V_{OL}	—	0.4	V
Input Leakage Current	\overline{RAS}	$I_{I(L)}$	-30	30	μA
	Others				
Output Leakage Current	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V}$, $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, Data out disabled	$I_{O(L)}$	-10	10	μA
Operating Current* ² (Average Power Supply Current)	MB8502D064AA-60	\overline{RAS} & \overline{CAS} cycling, $t_{RC} = \text{min.}$	—	1200	mA
	MB8502D064AA-70				
Standby Current* ² (Power Supply Current)	TTL Level	$\overline{RAS} = \overline{CAS} = \overline{PDE} = V_{IH}$	I_{CC2}	—	80
	CMOS Level				
Refresh Current #1* ² (Average Power Supply Current)	MB8502D064AA-60	$\overline{CAS} = V_{IH}$, $\overline{RAS} = \text{cycling}$, $t_{RC} = \text{min.}$	I_{CC3}	—	1200
	MB8502D064AA-70				
Fast Page Mode Current* ²	MB8502D064AA-60	$\overline{RAS} = V_{IL}$, $\overline{CAS} = \text{cycling}$, $t_{RC} = \text{min.}$	I_{CC4}	—	1147
	MB8502D064AA-70				
Refresh Current #2* ² (Average Power Supply Current)	MB8502D064AA-60	$\overline{RAS} = \text{cycling}$, \overline{CAS} -before- \overline{RAS} , $t_{RC} = \text{min.}$	I_{CC5}	—	1120
	MB8502D064AA-70				
Refresh Current #3 (Average Power Supply Current)	Self-Refresh; A_0 - A_{10} , B_0 , \overline{WE} , \overline{OE} , $\overline{PDE} \geq$ $V_{CC} - 2.1 \text{ V}$	I_{CC9}	—	30	mA

Notes: *1: Referenced to V_{SS} .

*2: I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, $V_{IL} > -0.3 \text{ V}$.

I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

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■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB8502D064AA-60		MB8502D064AA-70		Unit	Notes
			Min.	Max.	Min.	Max.		
1	Time Between Refresh	t _{REF}	—	32.8	—	32.8	ms	
2	Random Read/Write Cycle Time	t _{RC}	110	—	130	—	ns	
3	Read-Modify-Write Cycle Time	t _{RWC}	150	—	174	—	ns	
4	Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	ns	4, 7
5	Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	22	ns	5, 7
6	Column Address Access Time	t _{AA}	—	35	—	40	ns	6, 7
7	Output Hold Time	t _{OH}	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	t _{ON}	2	—	2	—	ns	
9	Output Buffer Turn Off Delay Time	t _{OFF}	—	20	—	22	ns	8
10	Transition Time	t _T	2	16	2	16	ns	
11	$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	ns	
12	$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	100000	70	100000	ns	
13	$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20	—	22	—	ns	
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	ns	
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	18	40	18	48	ns	9, 10
16	$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	—	17	—	ns	
17	$\overline{\text{CAS}}$ Hold Time	t _{CSH}	58	—	68	—	ns	
18	$\overline{\text{CAS}}$ Precharge Time (C-B-R Refresh)	t _{CPN}	10	—	10	—	ns	17
19	Row Address Setup Time	t _{ASR}	5	—	5	—	ns	
20	Row Address Hold Time	t _{RAH}	8	—	8	—	ns	
21	Column Address Setup Time	t _{ASC}	0	—	0	—	ns	
22	Column Address Hold Time	t _{CAH}	15	—	15	—	ns	
23	Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	33	—	33	—	ns	
24	$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	13	25	13	30	ns	11
25	Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	35	—	40	—	ns	
26	Column Address to $\overline{\text{CAS}}$ Lead Time	t _{CAL}	30	—	35	—	ns	
27	Read Command Setup Time	t _{RCS}	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	-2	—	-2	—	ns	12
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	—	0	—	ns	12
30	Write Command Setup Time	t _{WCS}	0	—	0	—	ns	13, 18
31	Write Command Hold Time	t _{WCH}	15	—	15	—	ns	
32	Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	33	—	33	—	ns	

(Continued)

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(Continued)

No.	Parameter	Symbol	MB8502D064AA-60		MB8502D064AA-70		Unit	Notes
			Min.	Max.	Min.	Max.		
33	\overline{WE} Pulse Width	tWP	15	—	15	—	ns	
34	Write Command to \overline{RAS} Lead Time	tRWL	20	—	22	—	ns	
35	Write Command to \overline{CAS} Lead Time	tCWL	15	—	17	—	ns	
36	D _{IN} Setup Time	tDS	-2	—	-2	—	ns	
37	D _{IN} Hold Time	tDH	20	—	20	—	ns	
38	Data Hold Time from \overline{RAS}	tDHR	35	—	35	—	ns	
39	\overline{RAS} to \overline{WE} Delay Time	tRWD	78	—	90	—	ns	18
40	\overline{CAS} to \overline{WE} Delay Time	tCWD	35	—	39	—	ns	18
41	Column Address to \overline{WE} Delay Time	tAWD	50	—	57	—	ns	18
42	\overline{RAS} Precharge Time to \overline{CAS} Active Time (Refresh Cycles)	tRPC	3	—	3	—	ns	
43	\overline{CAS} Setup Time (C-B-R Refresh)	tCSR	5	—	5	—	ns	
44	\overline{CAS} Hold Time (C-B-R Refresh)	tCHR	8	—	10	—	ns	
45	Access Time from \overline{OE}	tOEA	—	20	—	22	ns	7
46	Output Buffer Turn Off Delay from \overline{OE}	tOEZ	—	20	—	22	ns	8
47	\overline{OE} to \overline{RAS} Lead Time for Valid Data	tOEL	15	—	15	—	ns	
48	\overline{OE} Hold Time Referenced to \overline{WE}	tOEH	5	—	5	—	ns	14
49	\overline{OE} to Data in Delay Time	tOED	20	—	22	—	ns	
50	\overline{CAS} to Data in Delay Time	tCDD	20	—	22	—	ns	
51	D _{IN} to \overline{CAS} Delay Time	tDZC	-2	—	-2	—	ns	15
52	D _{IN} to \overline{OE} Delay Time	tDZO	-2	—	-2	—	ns	15
53	Fast Page Mode \overline{RAS} Pulse Width	tRASP	—	100000	—	100000	ns	
54	Fast Page Mode Read/Write Cycle Time	tPC	40	—	45	—	ns	
55	Fast Page Mode Read-Modify-Write Cycle Time	tPRWC	80	—	89	—	ns	
56	Access Time from \overline{CAS} Precharge	tCPA	—	40	—	45	ns	7, 16
57	Fast Page Mode \overline{CAS} Precharge Time	tCP	10	—	10	—	ns	
58	Fast Page Mode \overline{RAS} Hold Time from \overline{CAS} Precharge	tRHCP	40	—	45	—	ns	
59	Fast Page Mode \overline{CAS} Precharge to \overline{WE} Delay Time	tCPWD	55	—	62	—	ns	18
60	\overline{RAS} Pulse Width (Self Refresh)	tRASS	100	—	100	—	μs	19
61	\overline{RAS} Precharge Time (Self Refresh)	tRPS	110	—	125	—	ns	19
62	\overline{CAS} Hold Time (Self Refresh)	tCHS	-52	—	-52	—	ns	19

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- Notes: 1. An initial pause ($\overline{\text{RAS}}=\overline{\text{CAS}}=V_{\text{IH}}$) of 200 μs is required after power-up followed by any eight $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles are required instead of eight $\overline{\text{RAS}}$ cycles.
2. AC characteristics assume $t_{\text{T}} = 5 \text{ ns}$.
 3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
 4. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max.})$, $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max.})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
 5. If $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max.})$, $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max.})$, and $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{CAC} .
 6. If $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max.})$ and $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{AA} .
 7. Measured with a load equivalent to two TTL loads and 100 pF.
 8. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
 9. Operation within the $t_{\text{RCD}} (\text{max.})$ limit ensures that $t_{\text{RAC}} (\text{max.})$ can be met. $t_{\text{RCD}} (\text{max.})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}} (\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 10. $t_{\text{RCD}} (\text{min.}) = t_{\text{RAH}} (\text{min.}) + 2 t_{\text{T}} + t_{\text{ASC}} (\text{min.})$.
 11. Operation within the $t_{\text{RAD}} (\text{max.})$ limit ensures that $t_{\text{RAC}} (\text{max.})$ can be met. $t_{\text{RAD}} (\text{max.})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}} (\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 13. t_{WCS} is specified as a reference point only. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min.})$ the data output pin will remain High-Z state through entire cycle.
 14. Assumes that $t_{\text{WCS}} < t_{\text{WCS}} (\text{min.})$.
 15. Either t_{DZC} or t_{DZO} must be satisfied.
 16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{\text{CAS}}$ from "L" to "H"). Therefore, if t_{CP} become long, t_{CPA} also become longer than $t_{\text{CPA}} (\text{max.})$.
 17. Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh.
 18. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} , and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min.})$, the cycle is an early write cycle and D_{out} pin will maintain high impedance state throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min.})$, $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min.})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min.})$, and $t_{\text{CPWD}} \geq t_{\text{CPWD}} (\text{min.})$, the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL} , t_{CWL} , t_{RAL} and t_{CAL} specifications.
 19. Assumes that self refresh.

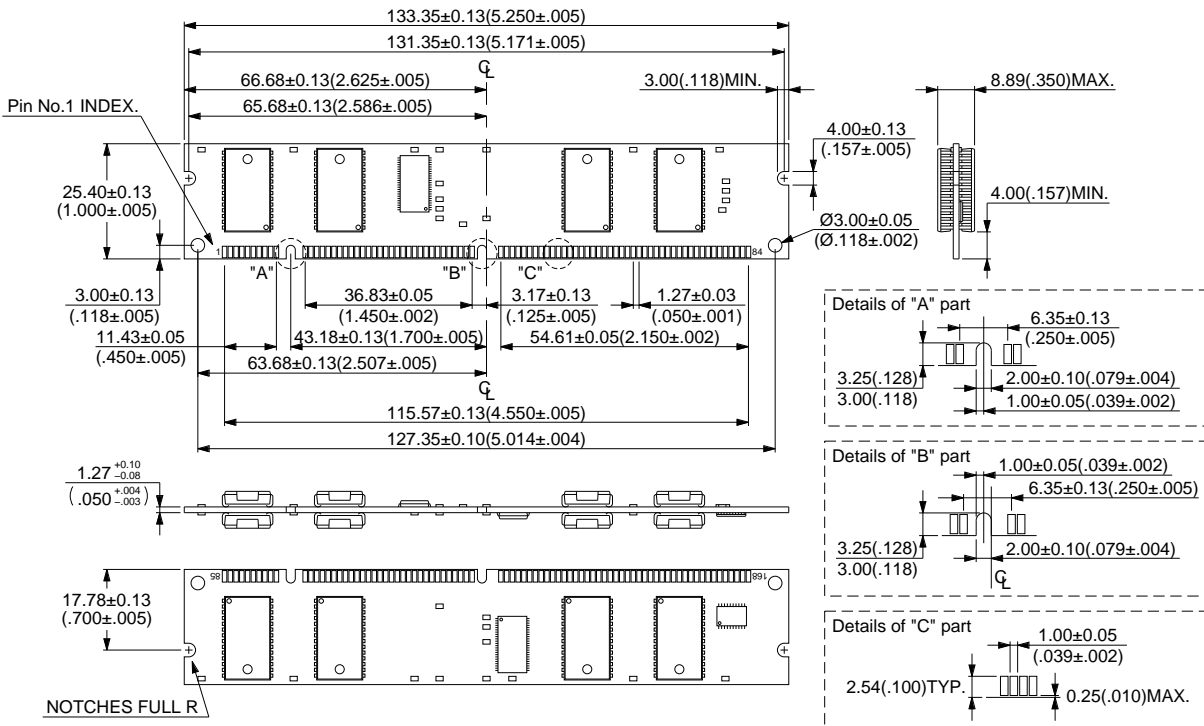
*Source: See MB8117800A Data Sheet for details on the electricals.

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■ PACKAGE DIMENSIONS

(Suffix: DG)

168 pin, Plastic DIMM
(MDS-168P-P06)



Dimensions in mm(inches).

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